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A Novel Approach and Implementation Concept For A Nanosatellite Backup on-Board Computer

H Venkatesh Kumar[1], Rohith S[2], Kasetty Ram Babu[3], Chikkarangaiah T R[4], Supreeth S[5]

[1,2,3,4]*Dept. Of Electronics and Communication Engineering, Nagarjuna College of engineering and Technology, Bangalore, Karnataka, India.*
[5]*School of CSE, REVA University, Bangalore, Karnataka, India.*
Email: venkateshkumar.h@gmail.com[1], rohithvjp2006@gmail.com[2], ramkasetty@gmail.com[3], chikkapr@gmail.com[4], supreeth1588@gmail.com[5]

**Corresponding author's E-mail: venkateshkumar.h@gmail.com*

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Abstract

STUDSAT-2 (STUDENT SATellite-2) is a one-of-a-kind satellite technology project undertaken by Indian undergraduate students. The aim of this project is to demonstrate the On-Board Computer's redundancy (OBC). The OBC subsystem is one of the many subsystems that make up the STUDSAT-2 satellite system. It is critical to the satellite's operation. Even a minor malfunction in this system could lead to the mission's complete failure. As a result, OBC redundancy management is required to overcome this. As a result, the proposed model of Backup On-Board Computer for STUDSAT-2 was planned and built by incorporating redundancy in both software and hardware, thus increasing the OBC's reliability.

Keywords: *STUDENT SATellite-2, Redundancy, On-board Computer, Watchdog Timer, Controller Area Network*

1. Introduction

This Artificial Satellites are man-made satellites that are placed into various orbits such as LEO (Lower Earth Orbit), MEO (Medium Earth Orbit), and GEO (Geosynchronous Earth Orbit) to gather data or communicate. STUDSAT is a student-led research project involving undergraduate students from seven separate universities. STUDSAT-1 was the first Pico-Satellite launched from Sriharikota onboard the PSLV C- 15 on July 12, 2010. The satellite's primary purpose is to conduct remote sensing and capture photographs of the earth's surface with a camera with a resolution of 90 meters, the highest resolution of any Pico-Satellite.

Following the successful launch of STUDSAT-1, the team is now working on STUDSAT– 2, which will carry on the legacy of STUDSAT-1. STUDSAT-2 is India's first twin nano- satellite (STUDSAT 2A and 2B), each weighing less than ten kilograms. Its aim is to show how to communicate between satellites and improve temporal resolution for remote sensing application

Figure 1: Inter-satellite Lnk

STUDSAT-2 is scheduled to launch with a beacon, telemetry data, and an Automatic Identification System (AIS) transceiver to demonstrate an inter-satellite connection and communicate with the ground station, as shown in Fig. 1. The deployable antennas on the spacecraft are expected to be installed on both satellites, 2A and 2B.

The design of a failure detection system for an OBC for STUDSAT-02 using an external watchdog timer is the subject of this principle. It entails redundancy design [1] and creation for OBC architecture, as well as software development for the microcontroller to detect errors and provide isolation, as well as fault tolerance for the STUDSAT-02.This principle is about designing a failure monitoring device for an OBC for STUDSAT-02 that uses an external watchdog timer. It involves OBC architecture redundancy design and construction, as well as microcontroller software development to detect errors and provide isolation, as well as fault tolerance for the STUDSAT-02.

The reset of the paper is organized as follows. Literature survey is discussed in section II. In section III overview of the proposed work is given. IMPLEMENTATION CONCEPT and proposed model details is given is section IV and V respectively. Section VI and Section VII IMPLEMENTATION CONCEPT and results and discussion is discussed. Conclusion of the paper is highlighted in Section VIII.

Literature Survey

In [1] the program memory of the on-board PC for satellite for space application suppressible to radiation effect is discussed. To address this issue, a dependable methodology to include a capacity unit with NOR Flash was proposed for space application. Also, the methodology dependent on triple measured repetition (TMR) was utilized to address the effect of radiation. Another impediment for TMR a memory framework is used by which to download the program into each chip. A TMR-Switch program downloading technique was proposed to beat it by setting download information way and controlling memory segments. In [2] is proposed a summary of On board Communication and dependencies and interaction between the on-board PC equipment, the on-board programming from ground is discussed. The highlights of the present on-board PCs is discussed nearby of their noteworthy advancement throughout the long time from the beginning of spaceflight up to now. Most recent framework on-chip processor designs are treated just as all ready PC significant segments. In [3], the handbook for Space Mission Engineering explain mission design, orbit selection to ground operation. SMAD III discusses updated technology with greater emphasis on small aircraft design. It also discusses on low-Earth orbit which is utilized in the task.

In this paper a novel idea of implementation concept for a nano satellite backup on-board computer is discussed.

Overview of The Proposed Work

A) SUB-SYSTEMS OFSTUDSAT-2

STUDSAT-2's entire system is divided into six subsystems for efficient execution. The On-Board Computer, also known as the satellite's brain, is in charge of all on-board operations. The Command and Data Handling Subsystem (C & DH) coordinates information flow between satellite subsystems. The Electronic Power System (EPS) is in charge of electrical power generation, storage, and distribution to subsystems. It takes the power produced by the solar panels and regulates and converts it to a charging voltage suitable for the storage batteries. The Attitude Determination & Control System (ADCS) is in charge of maintaining the target satellite altitude, as well as determining the satellite's location and correcting any deviations from the intended altitude.

The Skeleton is sent to the satellite by the mechanical subsystem. Design a structure with arrangement systems that have a stowed volume of 30x30x30 cm3 and a mass of less than 10 kg each. The satellite's communication connection with the ground station is established by the Communication Subsystem, which is made up of two parts: The space fragment that houses the satellite's onboard communication system as well as the ground station.

B) ON-BOARD COMPUTER(OBC)

The OBC is a special purpose onboard computer that monitors and controls the STUDSAT-2's real-time operations. It takes charge of the satellite shortly after launch and maintains it until the end of the satellite's operational existence. The primary role of the OBC is to provide autonomous control of all satellite subsystems. The OBC [2] also serves as a connection between the satellite bus and the radio link to the ground station. The 32-bit ARM Cortex M4-based STM32F407VGTx microcontroller with

built-in Digital Signal Processing (DSP) and Floating-Point Unit (FPU) is being considered for the twin Nano satellite

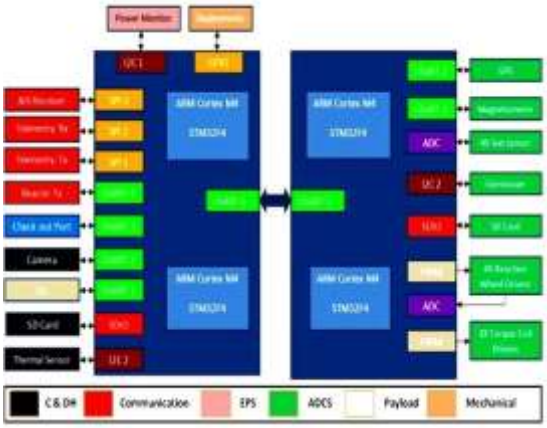

Figure 2: Architecture of On-Board Computer

The dual identical microcontroller is the core element of the OBC subsystem, as shown in Fig.2. Both microcontrollers are designed to perform ADCS and C&DH tasks simultaneously. It has different low power modes such as pause, standby, and sleep; the main benefit of these is that it allows the device to switch between these power modes using the real-time clock. The Backup-Onboard Computer is needed to track the following:

- Unpredictable hardware faults in the OBC trigger a malfunction in the satellite system, which could lead to mission failure.
- Environmental anomalies or any other physical variations in device subsystems and interfacing modules may cause failures in the hardware.

The nano satellite ensures OBC device redundancy at the system stage, as shown in Fig.3 the nano satellite's OBC architecture, where the master is in run mode and the redundant system is in standby mode. The CAN bus is used to communicate between the two, and the USART interface is used for IPC (inter-process communication) between the C&DH and ADCS subsystems. The watchdog timer is used to keep a constant eye on the system's errors.

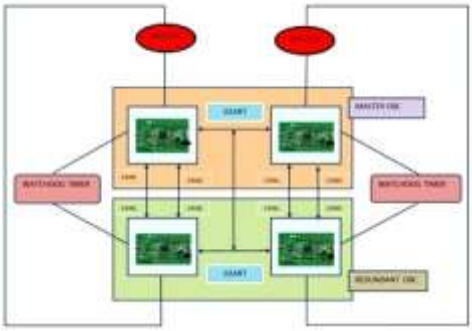

Figure 3: Architecture of Backup-Onboard Computer

Implementation Concept

Real time clock embedded on the redundant system wakes the system up from standby mode. OBC wakes up regularly to check master OBC activity. If there is a problem with Master OBC [3] redundant OBC will shutdown the satellite OBC operations.

The key benefit of using a watchdog timer is that it detects programming and equipment errors automatically and generates a time-out flag. In most cases, a watchdog timer relies on counters that act as a down clock. If the counter reaches zero before the main controller restarts, the main controller is likely to malfunction, and the processor reset flag is verified. In order to communicate The CAN (Controller Area Network) Protocol is used to communicate between different MCUs (Master Control Units). The MCUs communicate with one another over the CAN bus using a generic message.

•Both the primary devices, ADCS and C&DH, should be turned on and communicating with one another. The redundant systems should be placed into a deep state of sleep. When the primary system fails, the redundant system can take over the primary system's functions.

•To detect errors, the device employs an effective error detection [4] technique. The program can manage the observed faults correctly so that other satellite systems are not harmed. To communicate with each other, both systems should use the CAN Protocol.

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Proposed Model

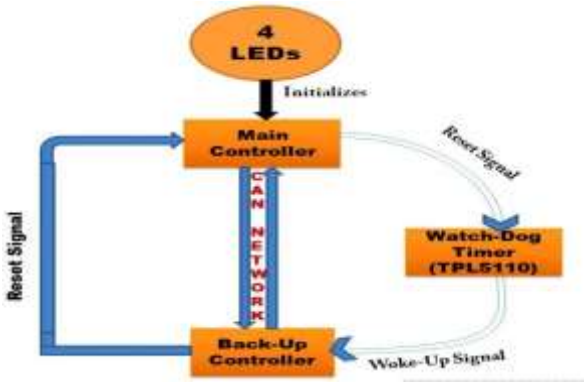

Figure 4: Proposed model of Backup On-Board Computer.

The key controller, as shown in Fig. 4, periodically resets the watchdog timer [5] to prevent it from elapsing or timing out during normal activity. The timer will elapse and produce a timeout signal if the main controller fails to reset the watchdog due to a hardware failure or a programming error

Corrective behaviors are triggered by the timeout signal. Until the watchdog timer receives a signal from WDT, the watchdog timer consumes less power than the active mode power consumption of the OBC. Back-up on board The computer is in sleep mode until it receives a signal from WTD, at which point it wakes up and begins sending and receiving data from the mainframe through the CAN trans receiver network. It normally includes putting the computer system in a safe state and restoring normal system activity in order to protect the satellite from problems and microcontroller.

HARDWAREIMPLEMENTATION:

Figure 5: STM32F407VG Discovery Broad, CAN, WDT, UART interconnection and implementation

The implementation of message transmission and reception using the CAN protocol (MCP2551) [6] in the STM32F407VG discovery board is shown in Fig.5. To detect the malfunctioning, an external watchdog timer is used. WDT (TPL5110) has three main pins. The Delay pin is used to set the counter value by attaching the appropriate resistor. The DONE pin of WDT is attached to the reset pin of the main onboard controller. When the DONE pin is not set, the DRV pin is set, which means it sends a wake-up signal to the backup controller. Using CAN transceivers between the boards, two STM32F407VG discovery boards are connected to demonstrate message transmission and reception. The CAN bus is made by serially connecting the CAN high and CAN low pins and using a terminator resistor. On the device panel, a UART module is attached to verify the display on an HTerm terminal window.

2. Results and Discussion

A) Master Obc Flow Chart

Initially, switch on the master OBC (see Fig.6). After the initialization and setup of all peripheral interfaces, the LED (Light Emitting Diode) blinks, and the watchdog timer is regularly refreshed by the master OBC, the LED activity starts. When errors or unforeseen bugs are discovered in STUDSAT-2 at that time, the main microcontroller fails to give the watchdog timer a reset signal. When the watchdog timer fails to refresh, the master will search for a hello message on CAN1 from the redundant OBC, and if one is received, it will send an acknowledgment message on the same line.

Figure 6: Flow Chart of Master OBC

If the message reception on CAN1 fails, the master will check the hello message on the CAN2 line and accept it once it has been received. When all three stages fail, the watchdog timer resets the master OBC, and the blinking LED operations resume.

Figure 7: Flow Chart of Redundant OBC

There are three levels of testing the master's activeness in Redundant OBC, as seen in the above Fig.7 procedure.Theinterruptfromthewatchdogtimerisfirstmonitoredbyastatus flag in level 1. If the flag status is null, the redundant OBC remains in deep sleep mode; otherwise, level 2 checking is

performed. In level 2, the redundant OBC waits for a random amount of time to receive a signal from the watchdog timer; if the signal is not received, it remains in sleep mode; if the signal is received, it sends a hello message to CAN1. If no acknowledgment is received, it will enter sleep mode and repeat the process from the beginning. If the acknowledgment message from the master on CAN1 is not received at level 3, then, on CAN 2, send a hello message to the master and wait for an acknowledgment message; if it is received, go to sleep mode and repeat from the first stage. If the master fails to accept the backup at all three stages, the redundant OBC should be reconfigured as the master and the process should be carried out in the desired order. Images of the primary and backup OBC controllers communicating successfully.

The redundant system is initially in sleep mode, but when the main system fails to reset the watchdog timer on a regular basis, it produces a wakeup signal. It wakes up from sleep mode after receiving a signal from the watchdog timer and begins communicating with the main device, which has been developed. The data is sent by the redundant machine if the acknowledgment is obtained, it returns to sleep mode, as shown in Figure 8. Every 30 seconds, this sequence will be repeated.

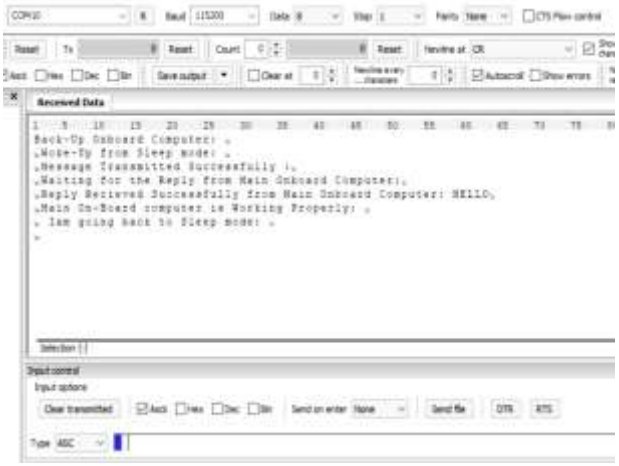

Figure 8: Snapshot of Redundant onboard controller

The transmission of a message from a CAN transreceiver can be seen in Figure 9. When the main onboard computer receives a message from the backup onboard computer, it shows the message "Message received successfully," and the received message from the backup onboard computer is "Hi." to display that the message has been received by the main backup machine It responds with a "working properly" acknowledgment, indicating that the process of transmitting and receiving the message is working properly by sending a "Hello" response, and the process continues. The acknowledgment is then sent to the backup controller.

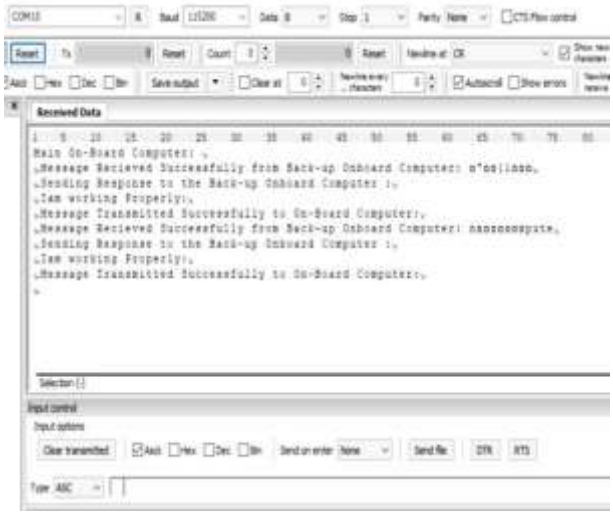

Figure 9: Output of Main onboard controller

When the main controller fails to submit an acknowledgment to the backup OBC, the operation must be restarted

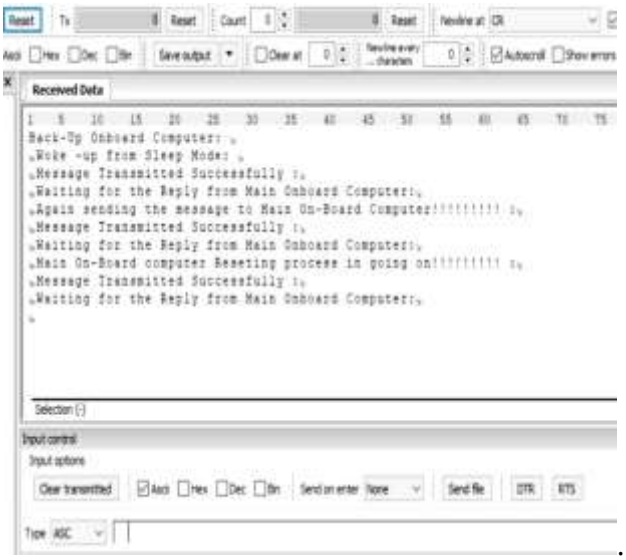

Figure 10: Backup On-board reset window

We can see from the above Fig.10 that the redundant device starts sending data. It returns to sleep mode if the acknowledgment is issued. If the main onboard computer does not respond, the redundant controller sends the request message to the main OBC again. If the acknowledgment is still not issued, the backup onboard computer system will be set to master.

Due to internal software or hardware failure, the main controller fails to reset the external watchdog timer, as shown in Fig.11. At that time, the watchdog timer wakes up the redundant controller from sleep mode, and the redundant controller acknowledges the request by sending ‘Hi Main' via the CAN trans receiver, but the main controller does not respond. By sending a reset order after two levels of failure, the redundant controller begins reconfiguring the main controller.

Figure 11: Main On-board reset window

4. Conclusion

This work demonstrates the fault tolerance and reconfigurable nature of an On-Board Computer for nano satellite missions, which will significantly extend mission duration. STUDSAT-2 has introduced OBC redundancy management for twin nano satellites with a watchdog timer, which has increased OBC efficiency by providing redundancy at the device, subsystem, and communication level interface. Backup and restore data are one of the most important enhancements. Since the redundant OBC does not need to wake up on a regular basis to check the health of the master OBC, the watchdog timer reduces power consumption. As a result, contact between the OBCs has a minimum delay (5-10ms) after the master OBC starts malfunctioning.

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